UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,380	10/30/2001	Hassan Hashemi	01CON288PC	4071

25700 7590 07/23/2004

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,380	HASHEMI ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *91-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *111-119* is/are allowed.

6)☒ Claim(s) *91-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 91, 95-105 and 107-110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwane (U.S. 5,719,750) in view of Currie et al (U.S. 4,446,477) and Bhattacharyya et al (U.S. 5,608,261).

As to claim 91, Iwane discloses in figures 1-10 an integrated module, comprising: a single interconnect substrate (10); a first active circuit chip (6a) bonded to the single interconnect substrate; a second active circuit chip (6c) interconnected to the single interconnect substrate; a first ground plane (3a) integral to the single interconnect substrate and operatively associated with the first active chip (6a); a second ground plane (3b) integral to the single interconnect substrate and operatively associated with the second active chip (6c); a first discrete component (8, Fig. 8) surface mounted on the single interconnect substrate, wherein the first ground plane (3a) is separated from the second ground plane (3b) (see col. 3, lines 58-62).

Iwane does not disclose a first active circuit chip (6a) is wire bonded to the single interconnect substrate. Currie et al discloses in figure 4, a first active circuit chip (11') is wire bonded to the single interconnect substrate. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane by having an active circuit chip which is wire bonded to the single

interconnect substrate as taught by Currie et al. One of ordinary skill in the art would have been motivated because using the wire bond method would provide a stronger bond for the connection and also reduce the amount of time (see col. 5, line 66 – col. 6, line 2 in Currie et al).

Iwane in view of Currie et al do not disclose a second discrete component situated on the single interconnect substrate. However, Bhattacharyya et al (U.S. 5,608,261) discloses in figure 3, a second discrete component (23) situated on the single interconnect substrate. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane in view of Currie et al by mounting/adding/situating another discrete component (second discrete component) on the single interconnect substrate as taught by Bhattacharyya et al. One of ordinary skill in the art would have been motivated because using another discrete component or second discrete component mounted/situated on the substrate would serve to filter frequency noise from the supply lines (see col. 2, lines 8-11 and col. 4, lines 55-65 in Bhattacharyya et al).

As to claim 95, Iwane discloses in figures 1-10 an integrated module, wherein the first discrete component (8) is a capacitor (see col. 6, lines 7-13).

As to claim 96, Iwane in view of Currie et al do not disclose the module comprising a second discrete component is a capacitor. Bhattacharyya et al (U.S. 5,608,261) discloses in figure 3 a module comprising a second discrete component (23) is a capacitor (see col. 4, lines 27-40). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane in view of Currie et al by mounting/adding/situating another discrete component

(second discrete component) is a capacitor on the single interconnect substrate as taught by Bhattacharyya et al. One of ordinary skill in the art would have been motivated because using another discrete component or second discrete component is a capacitor mounted/situated on the substrate would serve to filter frequency noise from the supply lines (see col. 2, lines 8-11 and col. 4, lines 55-65 in Bhattacharyya et al).

As to claim 97, Iwane discloses in figures 1-10 an integrated module, wherein the single interconnect substrate comprises a plurality of metal layers (1, 2a, 3a, 2b, 3b and 4) and a plurality of dielectric layers (5a, 5b, 5c, 5d and 5e) (see col. 3, lines 39-56).

As to claim 98, Iwane discloses in figures 1-10 an integrated module, wherein at least one of the plurality of metal layers (1, 2a, 3a, 2b, 3b and 4) defines a printed component ("inductor") (see col. 2, lines 48-50, and col. 3, line 58 - col. 4, line 10).

As to claim 99, Iwane discloses in figures 1-10 an integrated module, wherein the printed component including an inductor (see col. 2, lines 48-50).

As to claim 100, Iwane discloses in figures 1-10 an integrated module, wherein at least one of the plurality of metal layers (1, 2a, 3a, 2b, 3b and 4) defines one of the first and second ground planes (3a, 3b) (see col. 3, lines 57-62).

As to claim 101, Iwane discloses in figures 1-10 an integrated module, wherein the first active circuit chip (6a) comprises an RF section (see col. 5, lines 15-20, and col. 6, lines 50-60).

As to claim 102, Iwane discloses in figures 1-10 an integrated module, wherein the first active circuit chip (6a) comprises an IF section (see col. 2, lines 55-65 and col. 7, lines 27-30). It should be noted that since the ground plane (e.g., ground plane 3a) is connected to an inductor (see col. 2, lines 48-50), this means that the ground plane of first

active circuit chips including IF section (see col. 2, lines 55-65), thus it is considered that the first active circuit chip (6a) respectively comprises an RF section.

As to claim 103, Iwane discloses in figures 1-10 an integrated module further comprising at least one exposed conductive strip (see the conductive strip connected to left side of circuit chip 6a as shown in figure 6) formed on the single interconnect substrate and situated between the first and second active circuit chips (6a and 6c), the at least one exposed conductive strip electrically coupled to at least one of the first and second planes (see ground plane 3b which is connected to exposed conductive strip of 6c in figure 6).

As to claim 104, Iwane discloses in figures 1-10 an integrated module, wherein the first and second active circuit chips (6a, 6c) respectively comprise first and second RF sections (see col. 2, lines 55-65). It should be noted that since each ground plane (e.g., ground plane 3a or 3b) is connected to an inductor (see col. 2, lines 48-50), this means that each ground plane of first and second active circuit chips including an IF section (see col. 2, lines 55-65), thus it is considered that the first and second active circuit chip (6a, 6c) respectively comprise first and second RF sections.

As to claim 105, Iwane discloses in figures 1-10 an integrated module, wherein the first active circuit chip (6a) comprises an RF section and wherein the second active circuit chip (6c) comprises an IF section (see col. 6, lines 50-60).

As to claim 107, Iwane discloses in figures 1-10 an integrated module, wherein at least one of the plurality of metal layers (1-4) defines the first discrete component (8) (see col. 6, lines 5-14).

As to claim 108, Iwane discloses in figures 1-10 an integrated module, wherein the first discrete component is a capacitor (see col. 6, lines 5-14).

As to claims 109 and 110, Iwane in view of Currie et al do not disclose the plurality of metal layers defines the second discrete component, and wherein the second discrete component is a capacitor. Bhattacharyya et al (U.S. 5,608,261) discloses in figure 3 a module comprising a plurality of metal layers defines the second discrete component (23), and wherein the second discrete component is a capacitor (see col. 4, lines 27-40). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane in view of Currie et al by having/including another discrete component (second discrete component) is a capacitor and defined by the plurality of metal layers as taught by Bhattacharyya et al. One of ordinary skill in the art would have been motivated because using another discrete component or second discrete component is a capacitor would serve to filter frequency noise from the supply lines (see col. 2, lines 8-11 and col. 4, lines 55-65 in Bhattacharyya et al).

3. Claims 92-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwane (U.S. 5,719,750) in view of Currie et al (4,446,477) and Bhattacharyya et al (U.S. 5,608,261) as applied to claim 91 above, and further in view of Uchiyama (U.S. 6,356,333).

As to claim 92, Iwane discloses in figures 1-10 an integrated module, wherein the first discrete component (8) is surface mounted.

Iwane in view of Currie et al and Bhattacharyya et al do not disclose the first discrete component is surface mounted using a high-temperature solder. Uchiyama discloses in figure 1 an integrated module, wherein the first discrete component (6) is surface mounted on substrate (3) using a high-temperature solder (see col. 7, lines 1-11). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane in view of Currie et al and Bhattacharyya et al by using a high-temperature solder for surface mounting the discrete component on the substrate as taught by Uchiyama. One of ordinary skill in the art would have been motivated because using the high temperature solder for mounting the component on the substrate would reduce the amount of time ("short time") (see col. 10, lines 10-20 in Uchiyama), and also provide a reliability of the component and a good electrical contact between the component and the substrate.

Furthermore, the language of "using a high-temperature solder" in claim 92 is a process limitation in the product claim, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA 1965).

As to claims 93 and 94, Iwane in view of Currie et al and Bhattacharyya et al do not disclose the module further comprising solder mask area on the single interconnect substrate; and wherein the solder mask area is adjacent to the first discrete component. Uchiyama discloses in figure 1 an integrated module, wherein the module further comprising solder mask area (see element 13) on the single interconnect substrate (3); and wherein the solder mask area is adjacent to the first discrete component (6). Therefore, it would have been obvious to a person having ordinary skill in the art at the

time the invention was made to modify the module of Iwane in view of Currie et al and Bhattacharyya et al by having a solder mask area on the single interconnect substrate; and wherein the solder mask area is adjacent to the first discrete component as taught by Uchiyama. One of ordinary skill in the art would have been motivated because having a solder mask area on the single interconnect substrate would provide an electrical contact between the discrete component and the substrate by soldering the discrete component and the substrate together.

4. Claims 106 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwane (U.S. 5,719,750) in view of Currie et al (4,446,477) and Bhattacharyya et al (U.S. 5,608,261) as applied to claims 91 and 103 above, and further in view of Momose et al (U.S. 2004/0070024).

As to claim 106, Iwane in view of Currie et al and Bhattacharyya et al do not teach the first active circuit chip comprises a CMOS chip and the second active circuit chip comprises a GaAs chip. Momose et al teaches in col. 10, lines 4-20 a first active chip comprising a CMOS chip for increasing the operating speed and providing a high performance low-costly semiconductor device; and a second active circuit chip comprising a GaAs chip (see col. 7, line 57- col. 8, line 2) for use in analog integrated circuits communications. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Iwane in view of Currie et al and Bhattacharyya et al by replacing the first active circuit chip with the active circuit chip comprising a CMOS chip and the second active circuit chip with the active circuit chip comprising a GaAs chip as taught by Momose et al. One

of ordinary skill in the art would have been motivated because using a CMOS chip would increase the operating speed and provide a high performance low-costly semiconductor device for the module; and a GaAs chip for analog integrated circuits communications (see col. 7, line 57- col. 8, line 2, and col. 10, lines 4-20 in Momose et al).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT

7/13/04

DAVID ZARNEKE
PRIMARY EXAMINER
7/20/04